

RNA50C27AUS

CMOS System-Reset IC

R03DS0065EJ0200

Rev.2.00

Jul 03, 2012

Description

This IC facilitates complicated power-on and power-monitoring resets of microcomputers that require the 3.3-V and 1.8-V dual power supplies. It also facilitates change of delay time of reset signal by externally setting resistance and capacity for delay time. By employing complementary open-drain output, desired output such as open-drain output and CMOS output can be obtained.

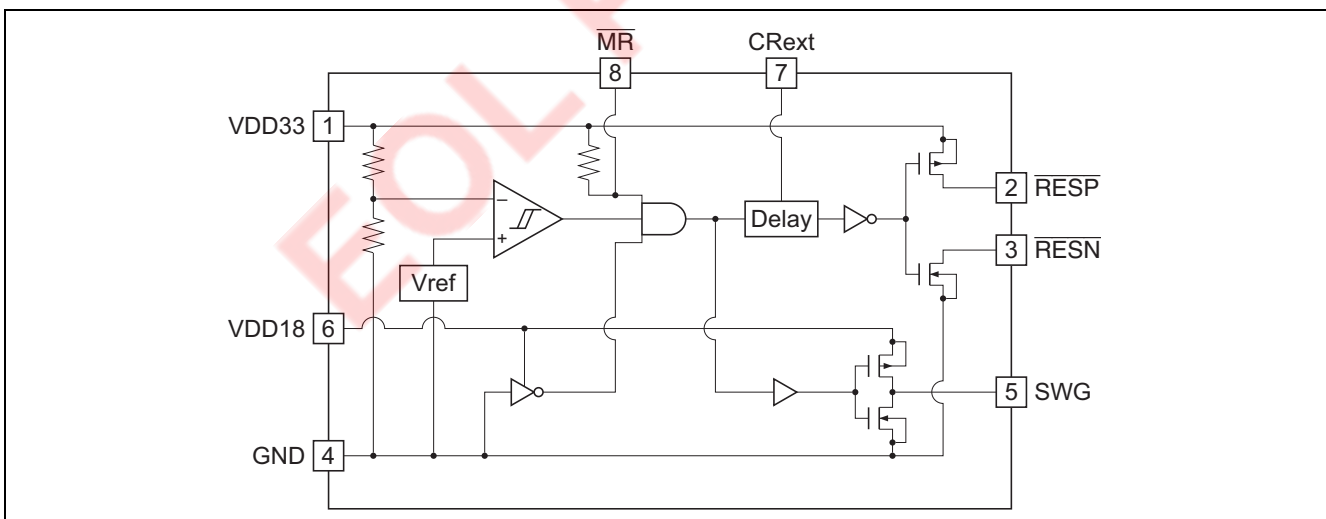
Functions

- 3.3-V detection voltage : 2.7 V
- Accuracy of 3.3-V detection voltage : $\pm 1.0\%$
- Hysteresis of 3.3-V detection voltage : 5% Typ.
- Open-drain/CMOS output
- 1.8-V PMOS drive output
- Ultra-small SSOP-8 package

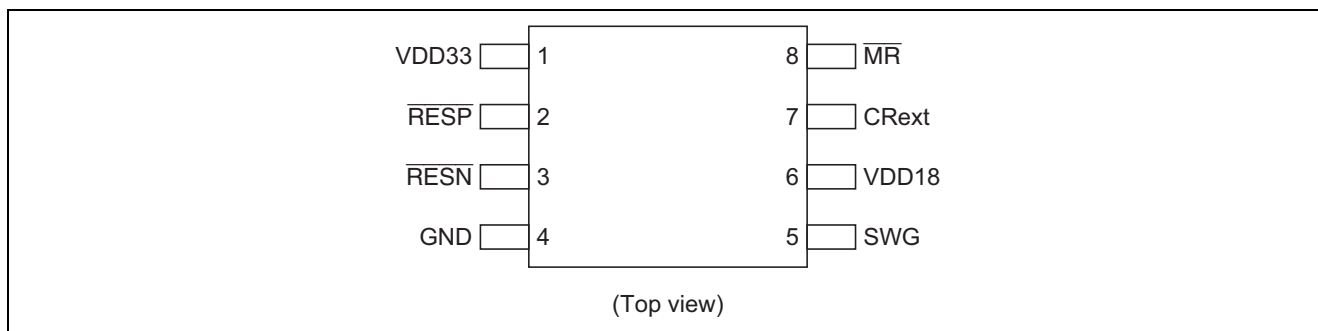
Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RNA50C27AUSEL-E	SSOP-8	PVSP0008KA-A	US	EL (3,000 pcs / Reel)	E (Sn-Bi)

Block Diagram



Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
1	VDD33	Input power supply pin for 3.3-V voltage. Recommended operating range is 2.7 to 3.6 V. Set the input voltage to 0.033 V/ μ s or less when starting up.
2	$\overline{\text{RESP}}$	Active-low reset signal output pin. By connecting to RESN pin, CMOS output can be used. If using open-drain, please connect pull-down resistor.
3	$\overline{\text{RESN}}$	Active-low reset signal output pin. By connecting to RESP pin, CMOS output can be used. If using open-drain, please connect pull-up resistor.
4	GND	GND pin
5	SWG	External PMOS gate control signal to be set between 1.8-V power supply and 1.8-V voltage input of microcomputer.
6	VDD18	Input power supply pin for 1.8-V voltage. Recommended operating range is 1.65 to 3.6 V.
7	CRext	Connecting pin for Rext resistance and Cext capacity that determine the delay time of reset signal. 3.3 k Ω or more is recommended for resistance. The delay time, t_{DLY} , is given by the following formula. $t_{\text{DLY}} = \text{Cext} \times \text{Rext} [\text{s}]$
8	$\overline{\text{MR}}$	Pin to provide reset manually. MR pin is pulled-up to VDD33 through internal resistor.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	VDD33	4.6	V
	VDD18	4.6	
Input voltage	V _I	-0.3 to VDD33+0.3	V
Output voltage	V _O	-0.3 to VDD33+0.3	V
Input current	I _I	20	mA
Output current	I _O	25	mA
Supply current	I _{DD}	25	mA
Power dissipation	P _T	273	mW
Storage temperature	T _{stg}	-55 to +125	°C

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Remarks
Supply voltage	VDD33	VTH33	—	3.6	V	
	VDD18	1.65	—	VDD33		
Input voltage	V _{MR}	0	—	VDD33	V	
Output voltage	V _O	0	—	VDD33	V	
	V _{OSWG}	0	—	VDD18		
External resistor	R _{ext}	3.3	—	—	kΩ	VDD33 = 3.3 V
External capacitor	C _{ext}	—	No limit	—		
Drivable capacitor	C _L	—	2200	—	pF	SWG output
Operating temperature	T _a	-40	—	85	°C	

Electrical Characteristics

DC Characteristics

(VDD33 = 3.3 V, VDD18 = 1.8 V, Ta = 25°C, C_{Rext}:R = 10 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Quiescent supply current		IDD33	0.75	1.5	4	μA	All outputs are open
		IDD18	0.25	0.5	2		
Detection voltage		VTH33	Typ×0.99	2.7	Typ×1.01	V	
		VTH _H	1.2	—	—		
		VTH _L	—	—	0.55		
Detection voltage temperature dependency		$\frac{\Delta V_{th33}}{V_{th} \cdot \Delta T_a}$	—	±100	—	ppm/°C	
Detection voltage hysteresis		V _{HYS}	VTH33×3%	VTH33×5%	VTH33×8%	V	
MR	Low-level input voltage	V _{IL}	—	—	VTH33×0.25	V	
	High-level input voltage	V _{IH}	VTH33×0.75	—	—	V	
	internal pull-up resistance	R _{MR}	—	T.B.D.	—	kΩ	
CMOS *1	Low-level output current	I _{OL}	7.5	15	30	mA	V _O = 0.5 V
	High-level output current	I _{OH}	5	10	20		V _O = VDD33 – 0.5 V
RESP	Output leakage current	I _{LEAK}	—	—	0.1	μA	RESN off
RESN	Output leakage current	I _{LEAK}	—	—	0.1	μA	RESP off
SWG	High-level output voltage	V _{OH}	1.7	—	—	V	V _O = open
	Output source current	I _{OH}	1.5	3	6	mA	V _O = VDD33 – 0.5 V
	Low-level output voltage	V _{OL}	—	—	0.1	V	V _O = open
	Output sink current	I _{OL}	0.2	0.35	0.55	mA	V _O = 0.5 V

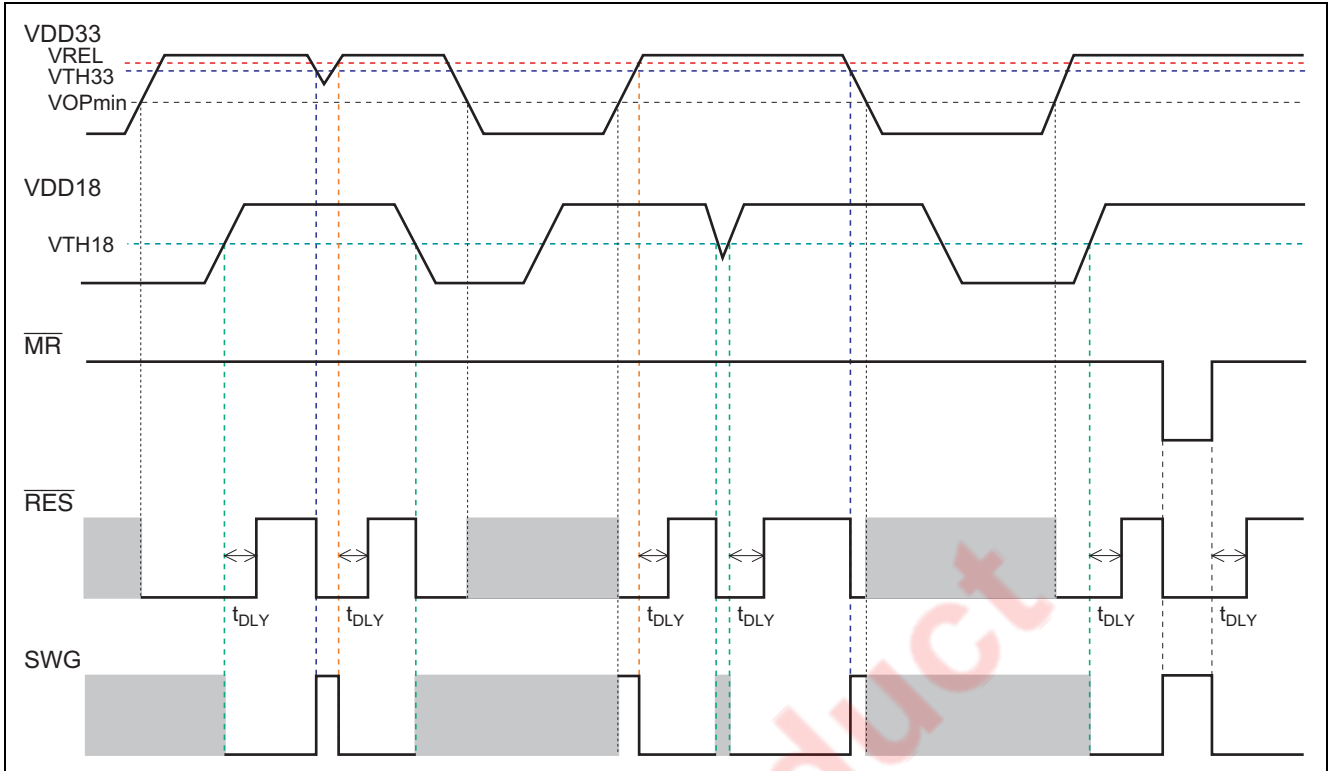
Note: When the voltage within $V_{IL} < V_{IN} < V_{IH}$ is applied to MR and VDD18 input by DC, oscillation may occur.

1. When RESP output and RESN short out and CMOS output is used.

AC Characteristics

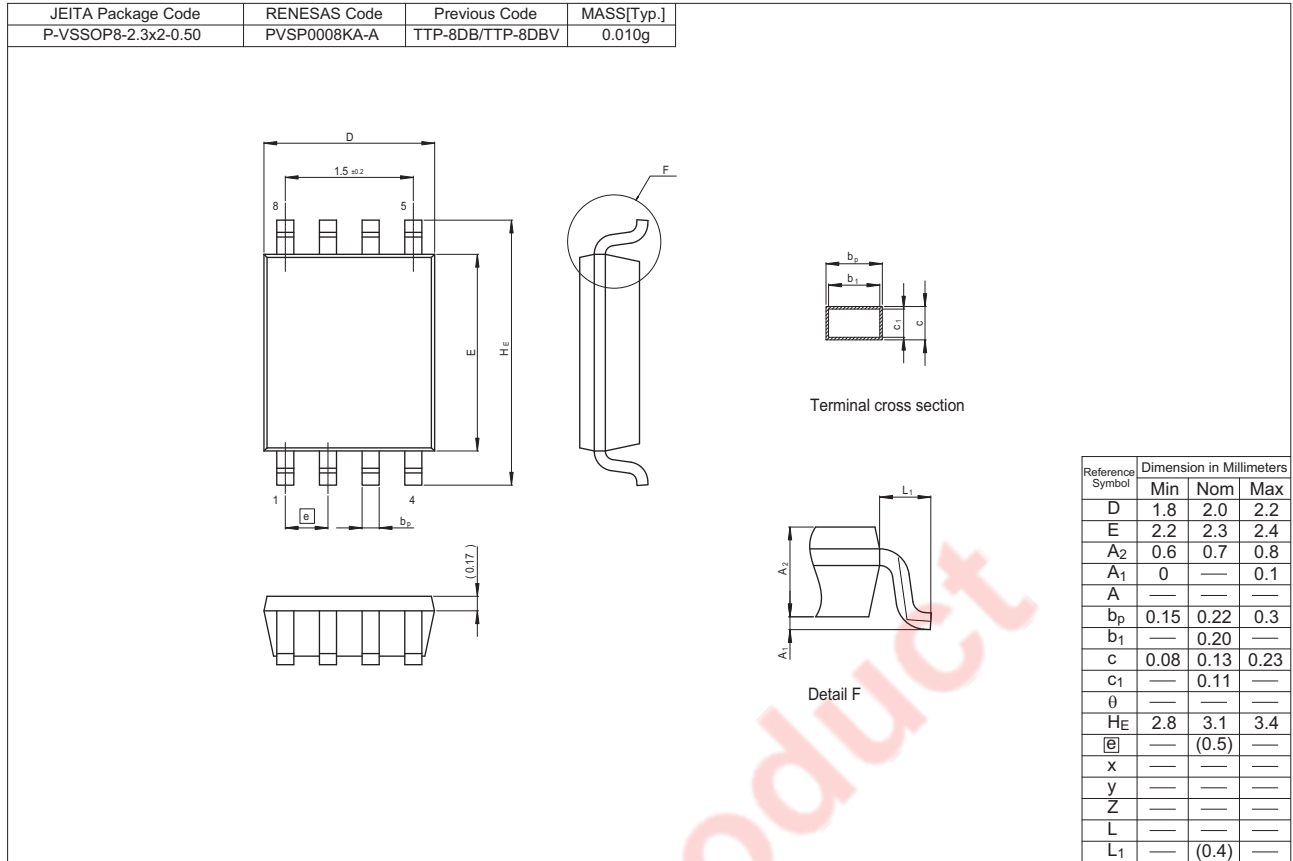
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
RESP	Propagation delay time	t _{PLH}	—	50	400	μs	C _L = 15 pF, C _{Rext} :C = open
		t _{PHL}	—	5	T.B.D.		
	Response time	t _r	—	5	T.B.D.	ns	C _L = 15 pF
		t _f	—	5	T.B.D.		
RESN	Propagation delay time	t _{PLH}	—	50	400	μs	C _L = 15 pF, C _{Rext} :C = open
		t _{PHL}	—	1.5	T.B.D.		
	Response time	t _r	—	5	T.B.D.	μs	C _L = 15 pF
		t _f	—	5	T.B.D.		
SWG	Propagation delay time	t _{PLH}	—	50	400	μs	C _L = 2200 pF
		t _{PHL}	T.B.D.	1.5	T.B.D.		
	Response time	t _r	T.B.D.	1.0	T.B.D.	μs	
		t _f	T.B.D.	7.6	T.B.D.		
Delay time		t _{DLY}	—	93	—	ms	C _{Rext} :C = 0.1 μF, R = 1 MΩ

Timing Chart

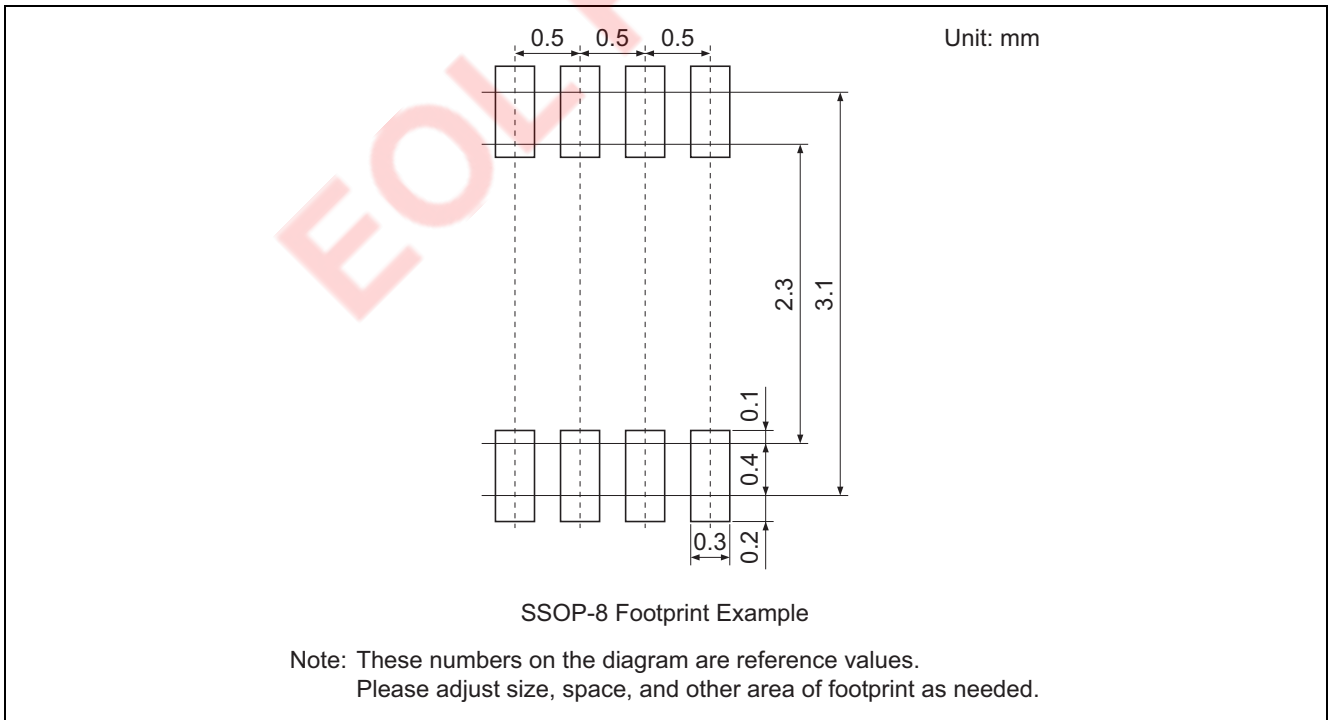


EOL Product

Package Dimensions



Footprint

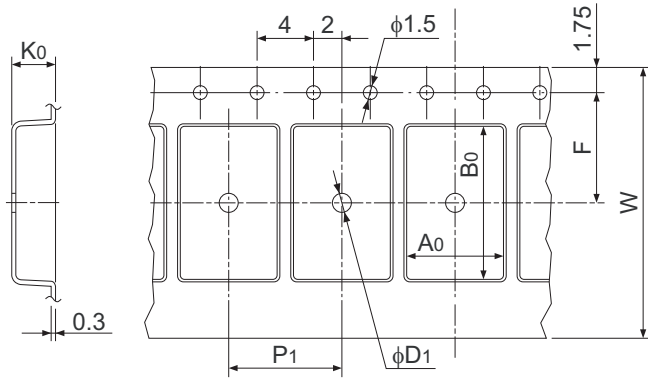


Taping and Reel Specifications

[Taping]

Unit: mm

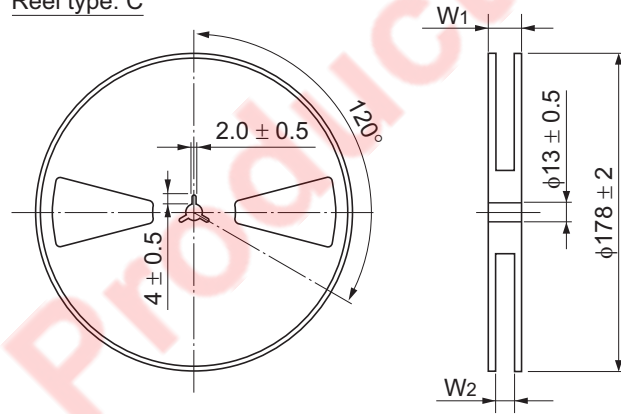
W	P1	A0	B0	K0	F	D1	Maximum Storage No.	Reel Type	Packing Form
8	4	2.25	3.4	1.0	3.5	1.05	3,000 IC/Reel	C	Non dry pack



[Reel]

Tape width: W	W1	W2
8	13.0	9.0

Reel type: C



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